

### Surface Mount Switching Diodes

**(P/b) Lead(Pb)-Free**

#### Features:

- \*Silicon Epitaxial Planar Diode
- \*Fast Switching Diodes
- \*500 mW Power Dissipation

#### Mechanical Data:

- \*Case : DO-35 Glass Case
- \*Weight : Approx 0.13 gram

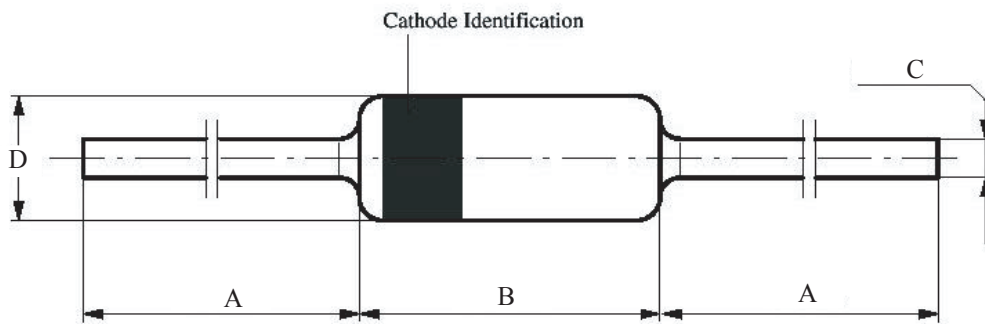
**SMALL SIGNAL  
SWITCHING DIODES  
150 m AMPERES  
100 VOLTS**



**DO-35**

### DO-35 Outline Dimensions

Unit:mm



DIM	A		B		C		D	
	Min	Max	Min	Max	Min	Max	Min	Max
<b>DO-35</b>	26.0	-	-	4.20	-	0.55	-	2.0

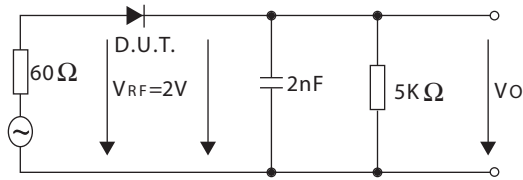
**Maximum Ratings** (  $T_A=25^\circ\text{C}$  Unless otherwise noted)

Characteristic	Symbol	1N4148/ 1N4448	Unit
Non-Repetitive Peak Voltage	$V_{RM}$	100	V
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	$V_{PWM}$ $V_{RWM}$ $V_R$	75	V
Average Rectified Output Current (1)	$I_o$	150	mA
Non-Repetitive Peak Forward Surge Current @ $t=1.0\mu\text{s}$	$I_{FSM}$	2.0	A
Power Dissipation	$P_d$	500	mW
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	300	K/W
Operating and Storage Temperature Range	$T_J, T_{STG}$	-65 to +175	$^\circ\text{C}$

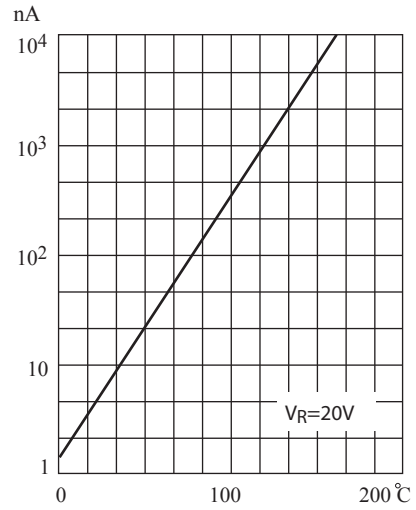
**Electrical Characteristics** (  $T_A=25^\circ\text{C}$  Unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Reverse Breakdown Voltage $I_R=100\mu\text{A}$	$V_{(BR)R}$	100	-	V
Forward Voltage 1N4148 $I_F=10\text{mA}$ 1N4448 $I_F=5\text{mA}$ $I_F=100\text{mA}$	$V_F$	0.62	1.0 0.72 1.0	V
Leakage Current $V_R=20\text{V}$ $V_R=75\text{V}$ $V_R=75\text{V}, T_J=150^\circ\text{C}$	$I_R$	-	25 5 50	nA
Junction Capacitance	$C_j$	-	4	PF
Reverse Recovery Time $I_F=10\text{mA}, I_R=1\text{mA}, V_R=6\text{V}, R_L=100\Omega$	$T_{rr}$	-	4	nS

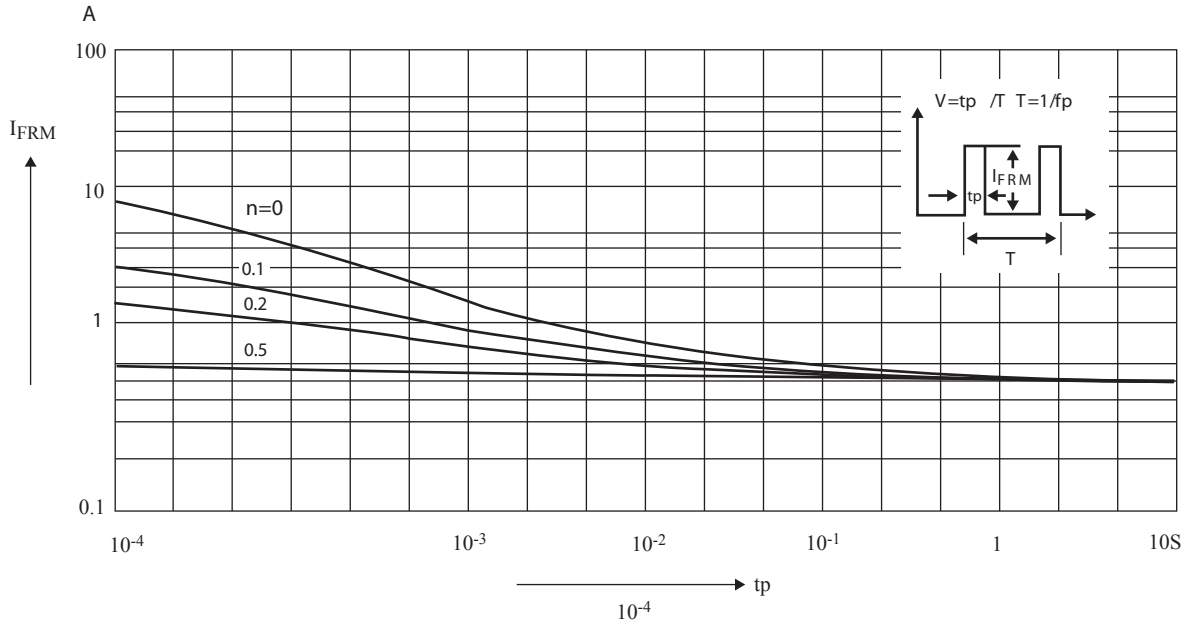
Note: 1.Valid Provided that device Terminals are Kept at Ambient Temperature.



**RECTIFICATION EFFICIENCY MEASUREMENT CIRCUIT**



**FIG 1, LEAKAGE CURRENT VERSUS JUNCTION TEMPERATURE**



**FIG 2, ADMISSIBLE REPETITIVE PEAK FORWARD CURRENT VERSUS PULSE DURATION**

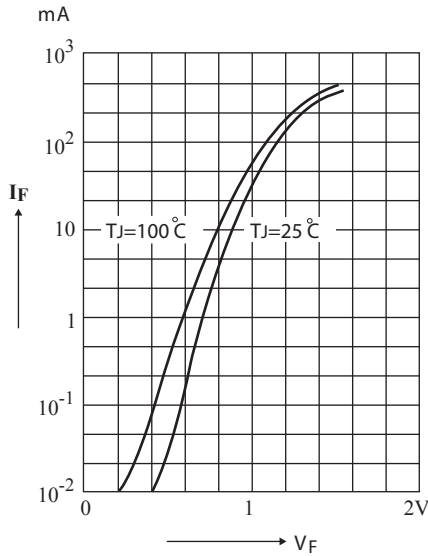


FIG 3, FORWARD CHARACTERISTICS

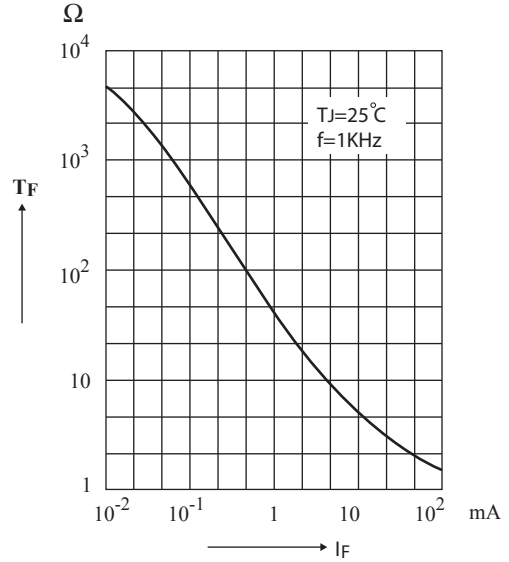


FIG 4, DYNAMIC FORWARD RESISTANCE VERSUS FORWARD CURRENT

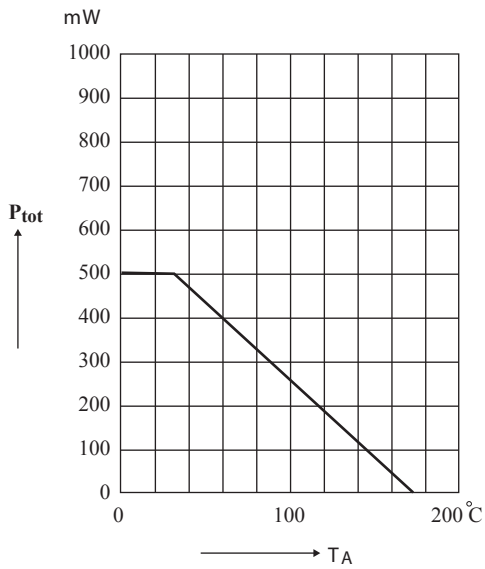


FIG 5, ADMISSIBLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

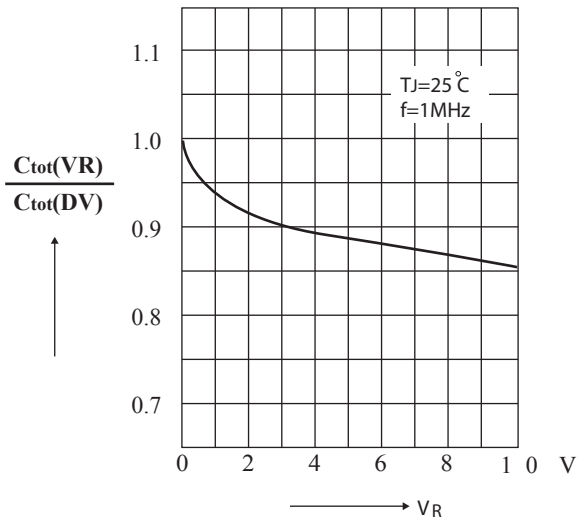


FIG 6, RELATIVE CAPACITANCE VERSUS VOLTAGE